CLAIMS

What is claimed is:

1. An apparatus, comprising:

a memory unit, said memory unit comprising a controller coupled to a memory core through an interface circuit, said interface circuit having a test data input that receives test data from said controller, said interface circuit having a system data input that receives data from a system, said interface circuit having a data output that is coupled to a data input of said memory core.

2. The apparatus of claim 1 wherein said controller further comprises an input for receiving a command.

3. The apparatus of claim 2 wherein said command further comprises a test command.

4. The apparatus of claim 3 wherein said test command further comprises a PRELOAD WRITE command.

5. The apparatus of claim 3 wherein said test command further comprises a PRELOAD READ command.

6. The apparatus of claim 3 wherein said test command further comprises a READ command.

7. The apparatus of claim 6 wherein said READ command has a field indicating less than a full word is to be read.

8. The apparatus of claim 3 wherein said test command further comprises a WRITE command.

9. The apparatus of claim 8 wherein said WRITE command has a field indicating less than a full word is to be written.

10. The apparatus of claim 2 wherein said command further comprises a configuration command.

11. The apparatus of claim 10 wherein said configuration command sets said controller into a transparent mode in which received test commands are ignored by said controller.

12. The apparatus of claim 10 wherein said configuration command sets said controller into a selected mode in which received test commands are executed by said controller.

13. The apparatus of claim 1 wherein said interface circuit couples said system data input through a multiplexer to said data input of said memory core.

14. The apparatus of claim 13 wherein said multiplexer has a second input coupled to said test data input.

15. The apparatus of claim 13 wherein said multiplexer has a select input coupled to a test enable signal, said multiplexer configured to enable said system data input if said test enable signal is inactive.

16. The apparatus of claim 13 wherein said memory core is a multi-port memory core.

17. The apparatus of claim 1 wherein said interface circuit couples said test data input to a register input.

18. The apparatus of claim 17 wherein said register has an output coupled to a multiplexer, said multiplexer having a second input that receives said test data input.

19. The apparatus of claim 18 wherein said multiplexer has a select input coupled to a controller output signal, said controller output signal configured to select said test data input if a port of said memory core that is coupled to said multiplexer output is a target port for a command.

20. The apparatus of claim 17 wherein said memory core is a multi-port memory core.

21. The apparatus of claim 1 wherein said controller further comprises an output for sending a command to a downstream controller in a daisy chain.

22. The apparatus of claim 1 in which said memory core further comprises a random access memory.

23. The apparatus of claim 1 in which said memory core further comprises a read only memory.

24. The apparatus of claim 1 in which said memory core further comprises a content addressable memory.

25. An, apparatus comprising:

a test unit;

a first memory unit having a controller coupled to a memory core, said controller having a test input coupled to an output of said test unit; and

a second memory unit having a second controller coupled to a second memory core, said second controller having a second test input coupled to an output of said controller.

26. The apparatus of claim 25 further comprising a last memory unit having a last controller coupled to a last memory core, said last controller having a last test input coupled to an output of an upstream controller.

27. The apparatus of claim 25 wherein said test unit further comprises an input coupled to an output of said last controller.

28. The apparatus of claim 25 wherein said last memory unit is said second memory unit, said last controller is said second controller, said last memory core is said second memory core, said upstream controller is said controller.

29. The apparatus of claim 25 further comprising a command at said test input.

30. The apparatus of claim 29 wherein said command further comprises a test command.

31. The apparatus of claim 30 wherein said test command further comprises a PRELOAD WRITE command.

32. The apparatus of claim 30 wherein said test command further comprises a PRELOAD READ command.

33. The apparatus of claim 30 wherein said test command further comprises a READ command.

34. The apparatus of claim 33 wherein said READ command has a field indicating less than a full word is to be read.

35. The apparatus of claim 30 wherein said test command further comprises a WRITE command.

36. The apparatus of claim 35 wherein said WRITE command has a field indicating less than a full word is to be written.

37. The apparatus of claim 29 wherein said command further comprises a configuration command.

38. The apparatus of claim 37 wherein said configuration command sets said controller into a transparent mode in which received test commands are ignored by said controller.

39. The apparatus of claim 38 in which said received test commands are sent from said controller output to said second test input while said controller is in said transparent mode.

40. The apparatus of claim 37 wherein said configuration command sets said controller into a selected mode in which received test commands are executed by said controller.

41. A method, comprising:

receiving a test command at a controller; and

executing said test command upon a memory core that is coupled to said controller, said test command sent from a second controller that is coupled to a second memory core, said second controller recognizing that said test command is not intended for said second controller.

42. The method of claim 41 wherein said controller addresses said memory core with an address supplied by said test command.

43. The method of claim 41 wherein said memory core is a multi-port memory core, said test command corresponding to a PRELOAD WRITE command in which data provided by said test command is entered at an input data port of said multi-port memory core.

44. The method of claim 43 wherein said input data port is specified by said test command.

45. The method of claim 41 wherein said memory core is a multi-port memory core, said test command corresponding to a PRELOAD READ command in which data read from an output port of said multi-port memory core by said controller is offered at an output of said controller.

46. The method of claim 45 wherein said output port is specified by said test command.

47. The method of claim 41 wherein said test command is a WRITE command in which data provided by said test command is written into said memory core by said controller.

48. The method of claim 41 wherein less than a full word is written into said memory core by said controller, said test command specifying which bytes of a full word are written.

49. The method of claim 41 wherein said test command is a READ command in which data read from said memory core by said controller is offered at an output of said controller.

50. The method of claim 49 wherein less than a full word is offered at said output of said controller, said test command specifying which bytes of a full word are to be offered.

51. The method of claim 41 in which said test command is initially sent by a test unit.

52. A method, comprising:

sending a configuration command from a test unit to a first of a plurality of a controllers coupled with said test unit in a daisy chain, each controller coupled to a different memory core.

53. The method of claim 52 wherein said configuration command sets said first controller to a transparent mode in which said first controller ignores subsequent test commands and forwards subsequent configuration commands to other controllers that are downstream in said daisy chain from said first controller.

54. The method of claim 52 wherein said configuration command sets said first controller to a selected mode in which said first controller executes subsequent test commands and forwards subsequent configuration commands to other controllers that are downstream in said daisy chain from said first controller.

55. The method of claim 54 further comprising sending a test command to said first controller.

56. The method of claim 55 wherein said first controller addresses a first memory core coupled to said first controller with an address supplied by said test command.

57. The method of claim 55 wherein said first memory core is a multi-port memory core, said test command corresponding to a PRELOAD WRITE command in which data provided by said test command is entered at an input data port of said multi-port memory core.

58. The method of claim 55 wherein said input data port is specified by said test command.

59. The method of claim 55 wherein said first memory core is a multi-port memory core, said test command corresponding to a PRELOAD READ command in which data read from an output port of said multi-port memory core by said controller is offered at an output of said first controller.

60. The method of claim 59 wherein said output port is specified by said test command.

61. The method of claim 55 wherein said test command is a WRITE command in which data provided by said test command is written into said first memory core by said first controller.

62. The method of claim 55 wherein less than a full word is written into said first memory core by said first controller, said test command specifying which bytes of a full word are written.

63. The method of claim 55 wherein said test command is a READ command in which data read from said first memory core by said first controller is offered at an output of said first controller.

64. The method of claim 63 wherein less than a full word is offered at said output of said first controller, said test command specifying which bytes of a full word are to be offered.

65. The method of claim 52 further comprising loading said memory cores with data reflective of a system having a software program that is desired to be executed.

66. The method of claim 65 further comprising reading data from said memory cores, said memory cores reflective of a system memory after a system failure.

67. The method of claim 66 wherein reading data further comprises dumping one or more of said memory cores.

68. The method of claim 65 wherein said data is reflective of a particular location of said software program.